REMARKS

Applicant has reviewed the Office Action mailed on March 23, 2006 as well as the art cited. Claims 1-5, 7-14, 32, 37 and 50 have been amended. Claims 1-50 are pending in this application.

Claim Objections

Claims 37-50 were objected to because of various informalities. The Applicant has amended Claim 37 as requested by the Examiner. Accordingly, the Applicant respectfully requests the withdrawal of the objections to claims 37-50.

Rejections Under 35 U.S.C. § 102

Claims 1-11 were rejected under 35 USC § 102(b) as being anticipated by Hall, (U.S. Patent No. 5,936,868).

Claims 1-50 were rejected under 35 USC § 102(b) as being anticipated by Yin, (U.S. Patent No. 6,298,469).

The Applicant has amended independent claims 1, 14 and 37 to further define the claims over the prior art.

Amended Claim 1 is as follows:

1. (Currently Amended) A method of designing devices in integrated circuits, the method comprising:

translating select device parameters in a first schematic database associated with a first process to device parameters in a second schematic database associated with a second process; and

displaying a design based on the device parameters in the second database.

The art references cited by the Examiner (Hall and Yin) are direct towards the downward scaling conversion or translation of layout data in a layout design. This is primarily applicable to digital/gate array circuits. Claim 1, as amended, includes the aspect of first and second schematic data bases. Schematic data bases are used to translate analog-type circuits and data. Neither the Hall nor the Yin reference teach the use of schematic data bases since neither the Hall nor Yin reference are directed towards analog-type circuits. The translation of layout data in a typical digital/gate array circuit, as described in Nall and Lin, is done by translating digital netlists and timing info, etc. The connectivity in these typical digital/gate array circuits is part of the netlist. Schematic data bases are typically not needed in digital/gate array circuits because there is either no schematic symbols used or the schematic symbols used only provide visual verification of the corresponding netlist and hence, do not effect connectivity. In contrast, in analog-type circuits, the schematic view contains symbols for devices such as resistors, BVJTs, MOS, that are not standardized. These symbols represent unique aspects of the process that need to be translated. Accordingly, since neither the Hall reference nor the Yin reference teach the aspect of schematic data bases as currently claimed in amended claim 1, the Applicant respectfully requests the withdrawal of the rejection of claim 1 and its dependant claims.

Amended claim 14 is as follows:

14. (Currently amended) A method of translating an integrated circuit design in a first process to a second process, the method comprising:

setting translations options; wherein setting translation options further comprises at least one of an option from a group of options comprising, setting select resistances to remain unchanged, setting select capacitances to remain unchanged and setting select geometries to remain unchanged;

reading original schematic information;

translating schematic information;

reading original layout information;

translating layout information; and

outputting parameters of translated schematic and layout information.

Amended claim 37 comprises:

37. (Currently amended) A computer-readable medium including instructions for simulating the design of an integrated circuit from one process to another process that when executed on a computer cause the computer to perform a method comprising:

processing translation options, wherein setting translation options further comprises at least one of an option from a group of options comprising, setting select resistances to remain unchanged, setting select capacitances to remain unchanged and setting select geometries to remain unchanged;

reading original schematic information;

translating schematic information;

reading original layout information;

translating layout information; and

outputting parameters of translated schematic and layout information.

Both claims 14 and 37 have been amended include the aspect "wherein setting translation options further comprises at least one of an option from a group of options comprising, setting select resistances to remain unchanged, setting select capacitances to remain unchanged and setting select geometries to remain unchanged." Neither the Yin nor the Hall reference teach any of the above options. As stated above, the Yin and Hall references relate to the downward scaling conversion or translation of layout data in a layout design. Accordingly, the Applicant respectfully requests the withdrawal of the rejection of claim 14 and 37 and there respective dependant claims.

Regarding the dependant claims, since the Applicant believes the claims are allowable for the above reasons a further response to all rejections to said claims in the office action may not have been addressed in this response. The Applicant however, retains the right to address said rejections if a further response is required.

CONCLUSION

Applicant respectfully submits that claims 1-50 are in condition for allowance and notification to that effect is earnestly requested. If necessary, please charge any additional fees or credit overpayments to Deposit Account No. 502432.

If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 332-4720.

Respectfully submitted,

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